REMARKS

An Office Action was mailed August 21, 2009. This response is timely. Any fee due with this paper, including any necessary extension fees, may be charged on Deposit Account 50-1290.

Summary

Claims 1, 3, 11, 13, 21, and claims 25-27 are being examined. Claims 1, 11, and 21 are the only independent claims.

By the foregoing, claims 1, 11, and 21 are amended. New independent claim 28 is presented. No new matter has been added.

Rejection under 35 U.S.C. §102(b) and 35 U.S.C. §103(a)

Claims 1, 3, 11, and 13 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,232,945 to Moriyama. Claims 25-27 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Moriyama in view of U.S. Patent No. 6,734,840 to Fukutofu. Independent claim 21 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Moriyama in view of JP 2001-249643 to Hirobumi. Thus, all claims stand rejected at least over Moriyama.

1. The cited art does not teach, disclose, or suggest the presently claimed invention wherein "*the resetting operation is completed before the writing period when the polarity of the data voltage is not inverted.*"

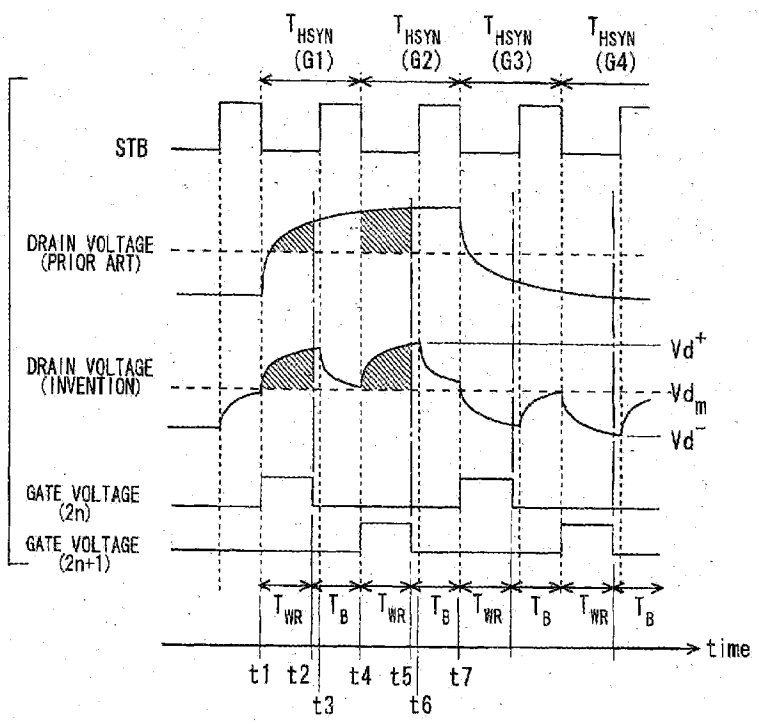
All independent claims now claim a resetting means that performs its resetting operation with reference to a latch signal,

> *wherein the resetting operation is completed before the writing period when the polarity of the data voltage is not inverted*

In the presently claimed invention, the resetting operation is carried out before the writing period T_{WR} where at least the polarity of the data, e.g., drain voltage is not inverted. As is evident from

Fig. 7 of the presently claimed invention, the polarity of the data voltage is not inverted from the time t1 to the time t6. At time t6, the data voltage is kept in the range Vd_m to Vd^+. Similarly, the drain voltage is not inverted from time t7 onward and the data voltage is kept in the range Vd_m to Vd^-.

FIG. 7



The resetting operation is then carried out at time t3 before the writing period T_{WR}. As the below detail of Fig. 7 shows, unlike the cited art, in the presently claimed invention, in the blanking period the data voltages are not applied. In fact, they are only applied during the writing periods. As is evident from Fig. 7, very advantageously, the polarity of the data voltage, i.e., drain voltage, is not inverted from t1 to t6, where the data voltage is kept from Vd_m to Vd^+.

Completing the resetting operation before the writing period when the polarity of the data voltage is not inverted presents significant advantages in image quality, because it prevents the formation of unwanted horizontal stripes without decreasing the luminance due to the total amount of charge written into the respective pixels when the LCD device is driven by the 2-H or more line inversion method. Doing so reduces the unwanted flicker known in the art

Moriyama fails to teach, disclose or suggest such an object of the invention. In Moriyama, an object is to makes it possible to display the non-display data in the non-display areas easily.

1:61-65 For example, image data for display size of 4 : 3 can be displayed on the screen of a display device having a display size of 16 : 9. As a result, Moriyama fails to teach, disclose, or suggest the resetting operation is carried out before the writing period where at least the polarity of the data voltage is not inverted.

Moriyama is cited for teaching a resetting circuit, which, as shown in Fig. 3, occurs in the blanking period. In Fig. 3, Moriyama teaches that the video signal ends abruptly at the beginning of the blanking period t1, but starts again during the blanking period Δt at time t2 at a new horizontal scanning period when the polarity has been inverted at time t2. In other words, the video signal has a middle point value between the positive and negative amplitudes in the Δt period that is shown in Fig. 3.

In the presently claimed invention, the resetting operation is one where the values of all data voltages, i.e., data lines, are brought closer to the middle point voltage between the positive and negative amplitudes. However, Moriyama teaches that a "resetting" wherein the non-display data, e.g., voltage for the black display is supplied to image signal bus lines in accordance with the reset signal. In fact, the non-display data is supplied only to the non-display areas in accordance with the reset signal; the non-display data is not supplied to the data lines.

Moriyama does refer to "polarity;" for example, "in the same horizontal period", solid display data, e.g., black display, which includes a precharge case, and "the image display section may have the same polarity (i.e., the same polarity along the horizontal direction of the screen)". However, Moriyama fails to disclose and teach the feature of the present invention that the relationship between the polarity of a horizontal period and the polarity of a next horizontal period, i.e., the same polarity along the vertical direction of the screen. Unlike this, in Moriyama, "resetting operation" means that non-display data, e.g., a voltage for black display, is supplied to the image signal bus lines in accordance with the reset signal. Therefore, the meaning of the resetting operation in the present invention is different from that of Moriyama.

Applicant respectfully submits that the middle point value in the Δt time period of Moriyama is not the resetting operation of the presently claimed invention. Rather, the middle point value prevents the OFF timing of the TFT controlled by the (N-1)th scanning line Y_{N-1} from being

delayed by the effect of the time constant of the Y_{N-1} scanning line. If the delay of the OFF timing of the TFT is not prevented, the image signal that is to be written into the Nth scanning line Y_N may be held by the pixel electrode corresponding to the (N-1)th scanning line Y_{N-1}.

Even so, Moriyama fails to teach the "resetting" without a polarity inversion. Indeed, Moriyama fails to disclose any examples of two or more H line inversions. Moriyama does teach that the polarity of the data voltage is inverted before and after the reset, but since Moriyama discloses digital logic circuits only, Moriyama inherently fails to teach, disclose or suggest "polarity inversion."

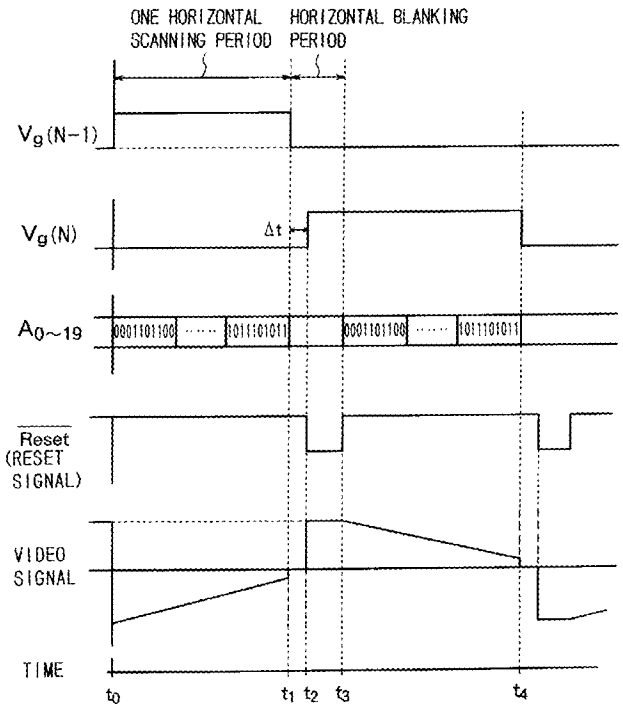


FIG. 3

The other cited art whether alone or in the combination with Moriyama as proposed does not teach, disclose, or suggest the claimed. Accordingly, the Examiner is respectfully requested to withdraw the rejection.

2. The cited art does not teach, disclose, or suggest the presently claimed invention *"wherein the data lines do not apply a subsequent data voltage to each of the pixels in the blanking period."*

All independent claims now claim a resetting means that performs its resetting operation *wherein the data lines do not apply a subsequent data voltage to each of the pixels in the blanking period.*

In the presently claimed invention, all the data lines are subjected to a resetting operation before the writing period T_{WR} regardless of the display area and the number of effective image data in each horizontal period.

As is evident from Fig. 10, all the data lines 18 (S1 to Sn) are reset by the reset signal SS. The resetting operation is carried out by resetting circuit 142 each horizontal synchronizing period $T_{HSYN,}$ as shown in Fig. 7, even if the 2-H dot inversion method shown in Fig. 4 is used. The resetting operation is realized by resetting all the outputs of the source driver circuit 14. Moreover, in the presently claimed invention the resetting operation is performed in each horizontal synchronizing period T_{HSYN} and is unrelated to the vertical synchronizing period.

In contrast, Moriyama teaches data lines corresponding to the non-display areas 503 and 504 shown in Fig. 4 or the non-display data display 905 and 906 shown in Fig. 14 are subjected to the resetting operation in the image invalid period in each horizontal synchronizing period. In this way, part of the data lines, which correspond to the display area 502 or 902 and which exceed the effective image data numbers, are reset.

In Moriyama, when the non-display data display areas 902 and 904 are respectively located at upper and lower positions of the display data display area 902, as shown in Fig. 14, two reset signals RESETY1 and RESETY2 are required . 12:54-61.

Further in Moriyama, the video signal line driving circuit 291 outputs the non-display data for the vertical scanning period, so that the non-display data can be written in a plurality of the horizontal pixel lines. 14:16-19. This means that when the non-display data display areas 902 and 904 are respectively located at upper and lower positions of the display data display area

902, the sampling pulses are outputted to the buffer amplified circuit 1007, so that the scanning voltage is outputted as shown in Fig. 16 in the vertical blanking period.

Thus, in Moriyama, the writing operation is carried out by selecting the non-display data from the source driver circuit,, not by resetting the outputs of the source driver circuit.

Accordingly, the Examiner is respectfully requested to withdraw the rejection.

In view of the remarks set forth above, this application is believed to be in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,

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